Govt Polytechnic Sundrenagar, Distt Mandi(H.P)

Lesson Plan (Theory)

Branch : Computer engineering **Semester: 4th**

Subject: Computer Organization & Architecture **Session: March-Aug,2021**

Teacher: Himani Vaidya **Class room: EC-101**

Sr. No	Number of Lecturers	Chapter/ Unit Description	Detail contents	References Recourses	Remarks
1	1-6 (06 hours)	**Unit-1 : Introduction**	Brief history of computers, Block Diagram of Digital Computers, Computer Organization, Computer Design and Computer Architecture, Von Neumann Architecture.	**R1**	
2	7-16 (10 hours)	**Unit-2 : Computer Arithmetic**	Addition and Subtraction with Signed-Magnitude Data - Hardware Implementation and Algorithm. Addition and Subtraction with 2's Complements Data - Hardware for 2's complement addition and subtraction, algorithm for adding and subtracting numbers in 2's complement representation. Multiplication Algorithms - Hardware Implementation for Signed-Magnitude Data, Booth Multiplication Algorithm.	**R1,R3**	
3	17-24 (08 hours)	**Unit-3 : Central Processing Unit**	Components of CPU, General Register Organization, Stack Organization - Register and Memory Stack, Reverse Polish Notation and Evaluation of Arithmetic Expressions; Instruction formats - Three Address Instructions, Two Address Instructions, One Address Instructions, Zero Address Instructions; Brief Introduction to RISC and CISC; Microprogrammed Vs Hardwired Control Units	**R1,R3,R4**	
4	25-32 (08 hours)	**Unit-4 : Memory Organization**	Memory Device Characteristics, Memory Hierarchy, Main Memory (RAM & ROM), Introduction to Associative Memory, Cache Memory - Locality of Reference, Hit Ratio, Writing into Cache - Write Through, Write Back	**R1,R2**	
5	33-40 (08 hours)	**Unit-5 : Input-Output Organization**	Peripheral Devices. Input-Output Interface - I/O Versus Memory Bus, Isolated versus Memory-Mapped I/O; Modes of Transfer - Programmed I/O, Interrupt-Initiated I/O and DMA.	**R1,R4**	

6	41-49 (08 hours)	Unit-6 : 8085 Microprocessor	Features, Block Diagram, Registers, Address Bus, Data Bus, Interrupts, Addressing Modes, Instruction Set (Introduction only), Memory and I/O Interfacing.	**R2,R4**	
7	50-55 (06 hours)	Unit-7 : Overview of Advanced Microprocessor Technologies	Parallel Processing, Pipelining, Vector Processing, Hyper Threading	**R1,R3**	

Teaching Resources:

R1: Computer System Architecture by M. Morris Mano, Pearson Education.

R2: Microprocessors Architecture, Programming and Applications with 8085 by R. Gaonkar, Penram International Publishing.

R3: Computer Architecture & Organization by J.P. Hayes, McGraw Hills.

R4: Fundamentals of Microprocessors and Microcontroller by B. Ram, Dhanpat Rai Publications.

Signature of Teacher

Approved

Signature of HOD

Govt Polytechnic Sundrenagar, Distt Mandi(H.P)
Practical Planning and coverage

Branch : Computer engineering **Semester: 4th**

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Teacher: Himani Vaidya **Lab: Network lab**

Practical No	Description of Practical	Reference for Procedure/writeup	Likely dates	Actual Dates	Signature
1	To add two 8-bit numbers resulting in 8 bits sum	Lab Manual	8/4/2021 to 17/4/2021		
2	To add two 8-bit numbers resulting in 16 bits sum.	Lab Manual	19/4/2021 to 24/4/2021		
3	To subtract two 8-bit numbers.	Lab Manual	26/4/2021 to 1/5/2021		
4	To multiply two 8-bit numbers	Lab Manual	3//5/2021 to 8/5/2021		
5	To find largest among two numbers.	Lab Manual	10/5/2021 to 15/5/2021		
6	To find the largest number in a data array	Lab Manual	17/5/2021 to 22/5/2021		
7	To find smallest among two numbers.	Lab Manual	24/5/2021 to 2/6/2021		
8	To find the smallest number in a data array	Lab Manual	3/6/2021 to 11/6/2021		
9	To sort a list of numbers.	Lab Manual	14/6/2021 to 19/6/2021		

Himani

Signature of Teacher

Approved

Signature of HOD